CHAPTER 5

Digitized Audio Telemetry Standard

List of Figures

Acronyms

CVSD	continuously variable slope delta
dB	decibel
Hz	hertz
kbps	kilobit per second
lsb	least significant bit
ms	millisecond
msb	most significant bit
PAM	pulse amplitude modulator
PCM	pulse code modulation

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CHAPTER 5

Digitized Audio Telemetry Standard

5.1   General

This chapter defines continuously variable slope delta (CVSD) modulation as the standard for digitizing audio and addresses the method of inserting CVSD encoded audio into a pulse code modulation (PCM) stream. Additional information and recommendations are provided in Appendix 5-A, which was extracted from the applicable sections of Military Standard 188-113, which has been canceled with no replacement.

Additional information regarding the insertion of the digitized voice signal into a PCM frame may be obtained in the documentation of US Patent 5,557,635.[1]

5.2   Definitions

For the purpose of this standard, the following definitions apply.

Band-Limited Audio: An audio signal (typically consisting of voice, tones, and sounds) that is limited to a subset of the audio spectrum. For most aircraft audio applications, the spectrum between 100 and 2300 hertz (Hz) is adequate.

Continuously Variable Slope Delta Modulation: The CVSD modulation is a method of digitizing a band-limited audio signal. The CVSD modulator is, in essence, a 1-bit analog-to-digital converter. The output of this 1-bit encoder is a serial bit stream, where each bit represents an incremental increase or decrease in signal amplitude and is determined as a function of recent sample history.

5.3   Signal Source

The signal to be encoded shall be a band-limited audio signal. The source of this signal may be varied. Some examples are microphones, communication systems, and tones from warning systems. This standard applies to <u>audio signals only</u>.

5.4   Encoding/Decoding Technique

The technique to encode and decode the band-limited audio signal is CVSD modulation. This technique is to be implemented in accordance with Appendix 5-A.

A CVSD converter consists of an encoder-decoder pair. The decoder is connected in a feedback path. The encoder receives a band-limited audio signal and compares it to the analog output of the decoder. The result of the comparison is a serial string of "ones" and "zeros." Each bit indicates that the band-limited audio sample's amplitude is above or below the decoded signal. When a run of three identical bits is encountered, the slope of the generated analog approximation is increased in its respective direction until the identical string of bits is broken. The CVSD decoder performs the inverse operation of the encoder and regenerates the audio signal.

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[1] Daniel T. Laird. Voice encode/decode subsystem in a system for acquisition of test data using pulse code modulation. US Patent 5,557,635, filed September 28, 1994 and issued September 17, 1996.

NOTE	A qualitative test of CVSD with a tactical aircraft intercom system yielded the following results: (1) intelligible, robotic sounding audio at 12 kilobits per second (kbps); (2) good quality audio at 16 kbps; and (3) audio quality did not significantly improve as the bit rate was increased above 32 kbps.

5.5   CVSD Encoder Output Bit Rate (CVSD Bit Rate)

The CVSD bit rate for encoding the band-limited audio signal is a function of the desired audio quality and the PCM format characteristics. The minimum and maximum CVSD bit rates will not be specified.

Appendix 5-A contains performance criteria for the CVSD encoder and decoder when operated at 16 or 32 kbps.

5.6   CVSD Word Structure

The digitized audio signal from the CVSD encoder's serial output shall be inserted into the PCM stream as shown in Figure 5-1. The most significant bit (msb) shall be the most stale sample (first in). The least significant bit (lsb) shall be the most recent sample (last in).
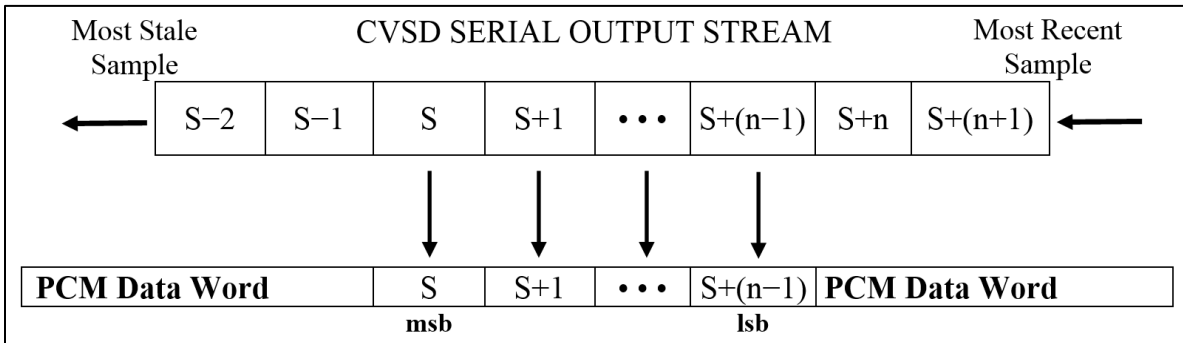
Figure 5-1.   Insertion of CVSD-Encoded Audio into a PCM Stream

5.7   CVSD Word Sample Rate

The CVSD word sample rate is dependent on the minimum desired CVSD bit rate, the PCM word length, and the PCM word sample rate. Once the CVSD word sample rate is determined, the actual CVSD bit rate can be calculated. The decoder must be run at the same CVSD bit rate as the encoder.

NOTE	Because of the nature of CVSD encoding, over and under sampling of the CVSD output will have unpredictable results.

NOTE	To simplify the reconstruction of the audio signal and minimize all encoding/decoding delays, it is STRONGLY recommended that the digitized audio words be inserted in the PCM stream at evenly spaced intervals.

5.8 CVSD Bit Rate Determination

The following discussion provides a procedure for determining the CVSD bit rate based on the desired minimum CVSD bit rate and information given in the host PCM format. Note that this procedure assumes the CVSD words are inserted in a class I PCM format with constant word widths and are not subcommutated. The CVSD bit rate can be obtained by multiplying the minor frame rate by the number of times the CVSD words appear in the minor frame by the word width used for the CVSD words in the minor frame. This relationship is expressed in equation (5-1).

$$\text{CVSD Bit Rate} = \text{Minor Frame Rate} \cdot \#\text{CVSD Words per Minor Frame} \cdot \text{Word Width} \qquad (5\text{-}1)$$

Knowing the details on the host PCM format, equation (5-1) contains two unknowns: CVSD bit rate and #CVSD words per minor frame. One of these unknowns must be chosen by the user; then the other one can be calculated. The recommended procedure is to choose the desired (target value) CVSD bit rate and solve equation (5-1) for #CVSD words per minor frame. This relationship is expressed in equation (5-2).

$$\#\text{CVSD WORDS PER MINOR FRAME}_{\text{CALCULATED}} = \frac{\text{DESIRED CVSD BIT RATE}}{\text{MINOR FRAME RATE} \cdot \text{WORD WIDTH}} \qquad (5\text{-}2)$$

Next, round up (if required) the result of equation (5-2) to the nearest integer. To satisfy the evenly spaced recommendation, round up (if required) to the nearest integer that divides evenly into the number of PCM words per minor frame.

Finally, for either case, substitute the result of equation (5-2) back into equation (5-1) to determine the actual CVSD bit rate. To illustrate this procedure, consider the following numerical example for determining the CVSD bit rate. An existing PCM format has the characteristics:

> Bit rate = 192,000 bits/second
> Word width = 12 bits/word
> Minor frame rate = 100 frames/second
> Words/ minor frame = 160 words/minor frame

To insert a serial CVSD bit stream with a desired (target value), CVSD bit rate of 16,000 bits/second will require the following procedure. Based on the information given, use equation (5-2) to calculate the #CVSD words per minor frame.

$$\#\text{CVSD WORDS PER MINOR FRAME}_{\text{CALCULATED}} = \frac{\text{DESIRED CVSD BIT RATE}}{\text{MINOR FRAME RATE} \cdot \text{WORD WIDTH}}$$

$$\#\text{CVSD WORDS PER MINOR FRAME}_{\text{CALCULATED}} = \frac{16\,000\ (bits/\text{sec})}{100\ (frames/\text{sec}) \cdot 12\ (bits/word)}$$

$$\#\text{CVSD WORDS PER MINOR FRAME}_{\text{CALCULATED}} = 13.3 \text{ words/frame}$$

Rounding up the #CVSD words per minor frame to the nearest integer yields 14. In this example, there are 160 PCM words in the minor frame. If the user needs to satisfy the evenly spaced criteria, then by inspection, the #CVSD words per minor frame will be rounded up to 16. For comparison, both cases will be substituted into equation (5-1) to yield the actual CVSD bit rate.

CASE 1: (unevenly spaced CVSD samples, NOT RECOMMENDED)

#CVSD WORDS PER MINOR FRAME $_{CALCULATED}$ = 14 $(words/frame)$

CVSD BIT RATE = MINOR FRAME RATE • #CVSD WORDS / MINOR FRAME • WORD WIDTH

CVSD BIT RATE $_{ACTUAL}$ = 100 $(frames/sec)$ • 14 $(words/frame)$ • 12 $(bits/word)$

CVSD BIT RATE $_{ACTUAL}$ = 16 800 $(bits/sec)$

CASE 2: (evenly spaced samples, RECOMMENDED)

#CVSD WORDS PER MINOR FRAME $_{CALCULATED}$ = 16 $(words/frame)$

CVSD BIT RATE = MINOR FRAME RATE • #CVSD WORDS PER MINOR FRAME • WORD WIDTH

CVSD BIT RATE $_{ACTUAL}$ = 100 $(frames/sec)$ • 16 $(words/frame)$ • 12 $(bits/word)$

CVSD BIT RATE $_{ACTUAL}$ = 19 200 $(bits/sec)$

APPENDIX 5-A

Continuously Variable Slope Delta Modulation

A.1.   General

The CVSD modulation is a nonlinear, sampled data, feedback system which accepts a band-limited analog signal and encodes it into binary form for transmission through a digital channel. At the receiver, the binary signal is decoded into a close approximation of the original analog signal. A typical CVSD converter consisting of an encoder and decoder is shown in Figure A-1 and Figure A-2.

Figure A-1.   Typical CVSD Encoder
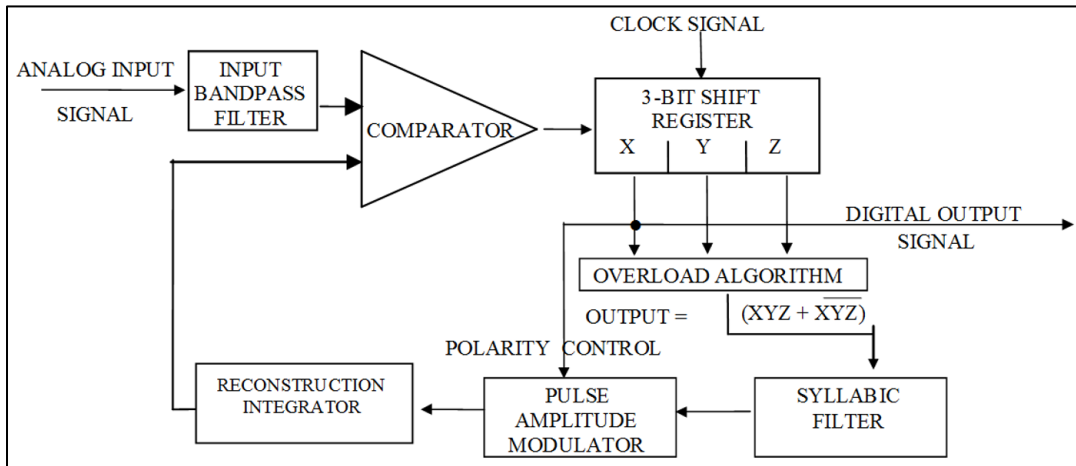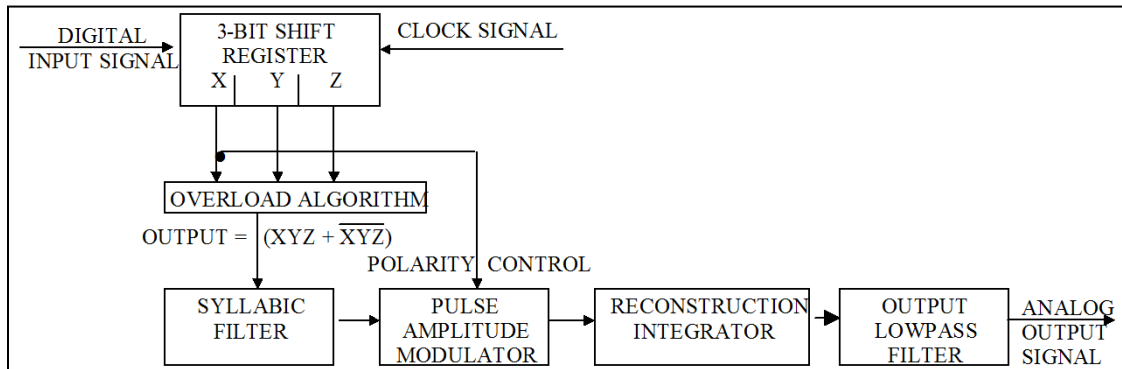

Figure A-2.   Typical CVSD Decoder

A.2.   General Descriptions

A general description of the delta modulation and the CVSD converter can be found in the following subparagraphs.

A.2.a.   Delta Modulation

Delta modulation is an A-D conversion technique resulting in a form of digital pulse modulation. A delta modulator periodically samples the amplitude of a band-limited analog

signal, and the amplitude differences of two adjacent samples are coded into n-bit code words. This nonlinear, sampled-data feedback system then transmits the encoded bit stream through a digital channel. At the receiving end, an integrating network converts the delta-modulated bit stream through a decoding process into a close approximation of the original analog signal.

A.2.b. <u>CVSD Converter</u>

A typical CVSD converter consists of an encoder and a decoder (see <u>Figure A-1</u> and <u>Figure A-2</u>). The analog input signal of the CVSD encoder is band-limited by the input band, pass filter. The CVSD encoder compares the band-limited analog input signal with an analog feedback approximation signal generated at the reconstruction integrator output. The digital output signal of the encoder is the output of the first register in the "run-of-three" counter. The digital output signal is transmitted at the clock (sample) rate and will equal "1" if the analog input signal is greater than or equal to the analog feedback signal at the instant of sampling. For this value of the digital output signal, the pulse amplitude modulator (PAM) applies a positive feedback pulse to the reconstruction integrator; otherwise, a negative pulse is applied. This function is accomplished by the polarity control signal, which is equal to the digital encoder output signal. The amplitude of the feedback pulse is derived by means of a 3-bit shift register, logic sensing for overload, and a syllabic lowpass filter. When a string of three consecutive ones or zeros appears at the digital output, a discrete voltage level is applied to the syllabic filter, and the positive feedback pulse amplitude increases until the overload string is broken. In such an event, ground potential is fed to the filter by the overload algorithm, forcing a decrease in the amplitude of the slope voltage out of the syllabic filter. The encoder and decoder have identical characteristics except for the comparator and filter functions.

The CVSD decoder consists of the input band pass filter, shift register, overload algorithm, syllabic filter, PAM and reconstruction integrator used in the encoder, and an output low-pass filter. The decoder performs the inverse function of the encoder and regenerates speech by passing the analog output signal of the reconstruction integrator through the low-pass filter. Other characteristics optimize the CVSD modulation technique for voice signals. These characteristics include the following.

   a. Changes in the slope of the analog input signal determine the step-size changes of the digital output signal.

   b. The feedback loop is adaptive to the extent that the loop provides continuous or smoothly incremental changes in step size.

   c. Companding is performed at a syllabic rate to extend the dynamic range of the analog input signal.

   d. The reconstruction integrator is of the exponential (leaky) type to reduce the effects of digital errors.

A.3.   Detailed Descriptions

The characteristics described in subparagraphs <u>A.3.a</u> through <u>A.3.i</u> are in addition to those specified in Section <u>A.5</u> and are for guidance only.

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A.3.a. Input Band Pass Filter

The input filter provides band-limiting and is typically a second- or higher-order filter (see Figure A-1).

A.3.b. Comparator

The comparator compares the band-limited analog input signal from the filter with the output signal of the reconstruction integrator (see Figure A-1). This comparison produces the digital error signal input to the 3-bit shift register. The transfer characteristic of the comparator is such that the difference between the two input signals causes the output signal to be driven to saturation in the direction of the sign of the difference.

A.3.c. 3-Bit Shift Register

The 3-bit shift register acts as a sampler which clocks the digital error signal from the comparator at the specified data signaling rate and stores the current samples and two previous samples of the error signal (see Figure A-1 and Figure A-2). The digital output signal is a binary signal having the same polarity as the input signal from the comparator at the time of the clock signal. The digital output signal is also the digital output of the encoder and is referred to as the baseband signal. Further processing for transmission such as conditioned diphase modulation may be applied to the baseband signal. It is necessary that the inverse of any such processing be accomplished and the baseband signal restored before the CVSD decoding process is attempted.

A.3.d. Overload Algorithm

The overload algorithm operates on the output of the 3-bit shift register (X, Y, Z) using the run-of-threes coincidence algorithm so that the algorithm output equals ($XYZ + \overline{XYZ}$) (see Figure A-1 and Figure A-2). The output signal is a binary signal at the clock signaling rate and is true for one clock period following the detection of three like bits and false at all other times.

A.3.e. Syllabic Filter

The syllabic filter acts as a low-pass filter for the output signal from the overload algorithm (see Figure A-1 and Figure A-2). The slope-voltage output of the syllabic filter is the modulating input to the PAM. The step-function response of the syllabic filter is related to the syllabic rate of speech, is independent of the sampling rate, and is exponential in nature. When the overload algorithm output is true, a charging curve is applicable. When this output is false, a discharging curve is applicable.

A.3.f. Pulse Amplitude Modulator

The PAM operates with two input signals: the output signal from the syllabic filter and the digital signal from the 3-bit shift register (see Figure A-1 and Figure A-2). The syllabic filter output signal determines the amplitude of the PAM output signal and the signal from the 3-bit shift register is the polarity control that determines the direction, plus or minus, of the PAM output signal. The phrase "continuously variable" in CVSD is derived from the way the PAM output signal varies almost continuously.

A.3.g. Reconstruction Integrator

The reconstruction integrator operates on the output signal of the PAM to produce an analog feedback signal to the comparator (or an output signal to the output low-pass filter in the receiver) that is an approximation of the analog input signal (see Figure A-1 and Figure A-2).

A.3.h. Output Low-Pass Filter

The output filter is a low-pass filter having a frequency response that typically has an asymptotic rolloff with a minimum slope of 40 decibels (dB) per octave, and a stopband rejection that is 45 dB or greater (see Figure A-2). The same output filter characteristic is used for encoder digital output signals of either 16 or 32 kbps.

A.3.i. Typical CVSD Decoder Output Envelope Characteristics

For a resistance/capacitance circuit in the syllabic filter with time constants of 5 milliseconds (ms) for both charging and discharging, the envelope characteristics of the signal at the decoder output are shown in Figure A-3. For the case of switching the signal at the decoder input from the 0 percent run-of-threes digital pattern to the 30 percent run-of-threes digital pattern, the characteristic of the decoder output signal follows the resistance/capacitance charge curve. Note that the number of time constants required to reach the 90 percent charge point is 2.3, which gives a nominal charge time of 11.5 ms.
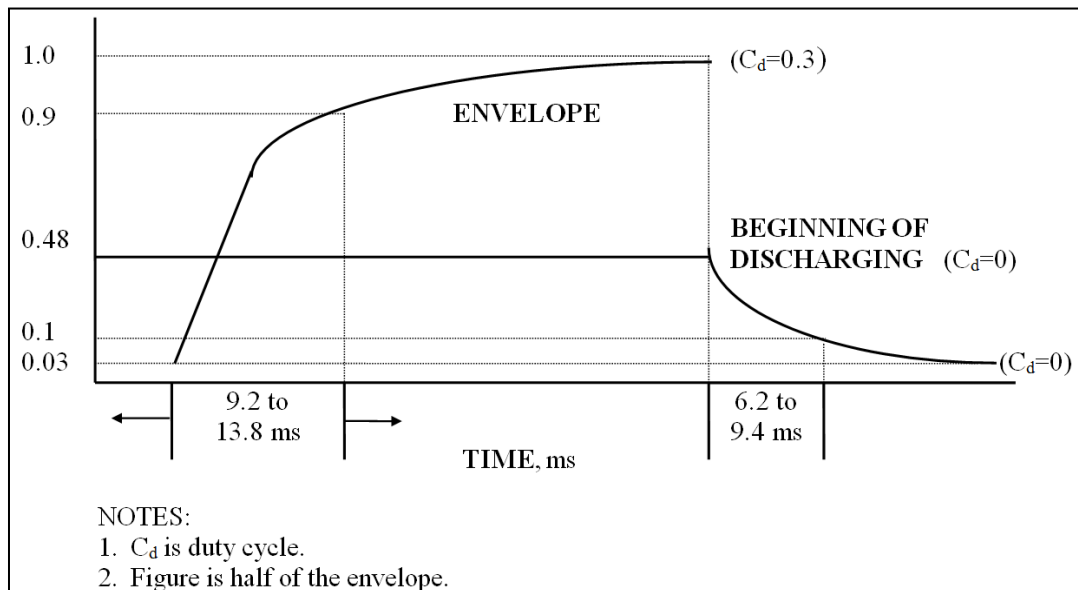

Figure A-3.   Typical Envelope Characteristics of the Decoder Output Signal for CVSD

When switching the other way (from the 30 percent pattern to the 0 percent pattern), the amplitude at the beginning of discharging is, at the first moment of switching, higher (by a factor of 16) than the final value which is reached asymptotically. The final value equals −24 dBm0, that is, 0.03. Therefore, the amplitude at the beginning of discharging is 0.48 (percent run-of-threes = 0). Note that the number of time constants required to reach the 10 percent point on the discharge curve is 1.57, which gives a nominal discharge time of 7.8 ms.

A.4.   Reference Level

The decoder analog output level with the 16 and 32 kbps, 30 percent run-of-threes reference digital pattern applied to the decoder input shall be the reference level for the CVSD requirements of this standard and shall be designated 0 dBm0 (see Subparagraph A.5.i(1)).

A.5.   CVSD Characteristics

The characteristics of CVSD are described in the following subparagraphs.

A.5.a.   Input and Output Impedances

The analog input and output impedances for CVSD converters are not standardized. These impedances depend upon the application of the converters.

A.5.b.   Data Signaling Rates

The CVSD converter shall be capable of operating at 16 and 32 kbps.

A.5.c.   Input and Output Filters

The analog input shall be band pass filtered. The analog output shall be low pass filtered.

NOTE	Details of input and output filers, consistent with the CVSD performance requirements of this standard, will be determined in applicable equipment specifications based on validated requirements

A.5.d.   Overload Algorithm

A 3-bit shift register shall be used for the CVSD encoder and decoder (see Figure A-1 and Figure A-2). The overload logic shall operate on the output of this shift register using the run-of-threes coincidence algorithm. The algorithm output signal shall be a binary signal at the data-signaling rate. This signal shall be true for one clock period following the detection of three like bits (all 0s or all 1s) and false at all other times.

A.5.e.   Compression Ratio

The compression ratio shall be nominally 16:1 with a maximum of 21:1 and a minimum of 12:1. The maximum slope voltage shall be measured at the output of the syllabic filter for a 30 percent run-of-threes digital pattern. The minimum slope voltage shall be measured at the output of the syllabic filter for a 0 percent run-of-threes digital pattern.

A.5.f.   Syllabic Filter

The syllabic filter shall have a time constant of 5 ms ±1. The step function response of the syllabic filter shall be exponential in nature. When the output of the overload algorithm is true, a charge curve shall be applicable. When the output of the overload algorithm is false, a discharge curve shall be applicable.

A.5.g.   Reconstruction Integrator Time Constant

The reconstruction integrator shall have a time constant of 1 ms ±0.25.

A.5.h.   Analog-to-Digital Conversion

An 800-Hz ±10 signal at a 0 dBm0 level applied to the input of the encoder shall give a duty cycle of 0.30 at the algorithm output of the encoder shown in Figure A-1.

A.5.i.   Digital-to-Analog Conversion

The characteristics of a digital-to-analog conversion are described in the following subparagraphs.

A.5.i(1)   Relation of Output to Input

With the applicable reference digital patterns of Table A-1 applied to the digital input of the decoder as shown in Figure A-4, the analog output signal shall be 800 Hz ±10 at the levels shown in Table A-1, measured at the decoder output. These digital patterns, shown in hexadecimal form, shall be repeating sequences.

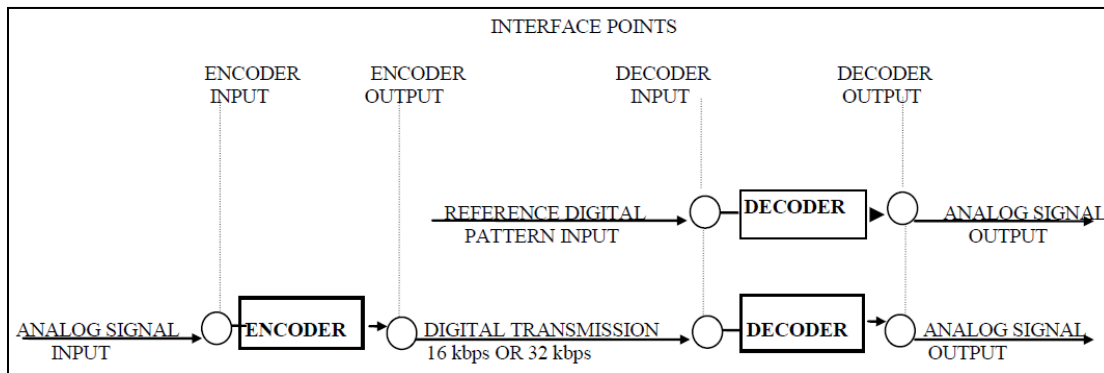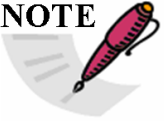| Table A-1. Decoder Reference Digital Patters for CVSD			
Data Signaling Rate (kbps)	Digital Pattern	Run-of-threes (percent)	Output (dBm0)
16	DB492	0	−24±1
32	DB54924AB6	0	−24±1
16	FB412	30	0±1
32	FDAA10255E	30	0±1

Figure A-4.   Interface Diagram for CVSD Converter

A.5.i(2)   Conversion Speed

When the decoder input is switched from the 0 percent run-of-threes digital pattern to the 30 percent run-of-threes digital pattern, the decoder output shall reach 90 percent of its final value within 9 to 14 ms. When the decoder input is switched from the 30 percent run-of-threes digital pattern to the 0 percent run-of-threes digital pattern, the decoder output shall reach 10 percent of the 30 percent run-of-threes value within 6 to 9 ms. These values shall apply to both the 16- and 32-kbps data signaling rates.

A.5.j.   CVSD Converter Performance

The characteristics specified in subparagraphs A.5.j(1) through A.5.j(7) apply to one CVSD conversion process obtained by connecting the output of an encoder to the input of a decoder (see Figure A-4).

NOTE 🖊	Test signal frequencies that are submultiples of the data signaling rate shall be avoided by offsetting the nominal test frequency slightly; for example, an 800-Hz test frequency could be offset to 804 Hz. This test frequency offset will avoid nonlinear distortion, which can cause measurement difficulties when CVSD is in tandem with PCM.

A.5.j(1)   Companding Speed

When an 800-Hz ±10 sine wave signal at the encoder input is switched from −24 dBm0 to 0 dBm0, the decoder output signal shall reach 90 percent of its final value within 9 to 14 ms.

A.5.j(2)   Insertion Loss

The insertion loss between the encoder input and the decoder output shall be 0 dB ±2 dB with an 800 Hz ±10, 0 dBm0 input to the encoder.

A.5.j(3)   Insertion Loss vs. Frequency Characteristics

The insertion loss between the encoder input and decoder output, relative to 800 Hz ±10 measured with an input level of −15 dBm0 applied to the converter input, shall not exceed the limits indicated in Table A-2 and shown in Figure A-5 and Figure A-6.

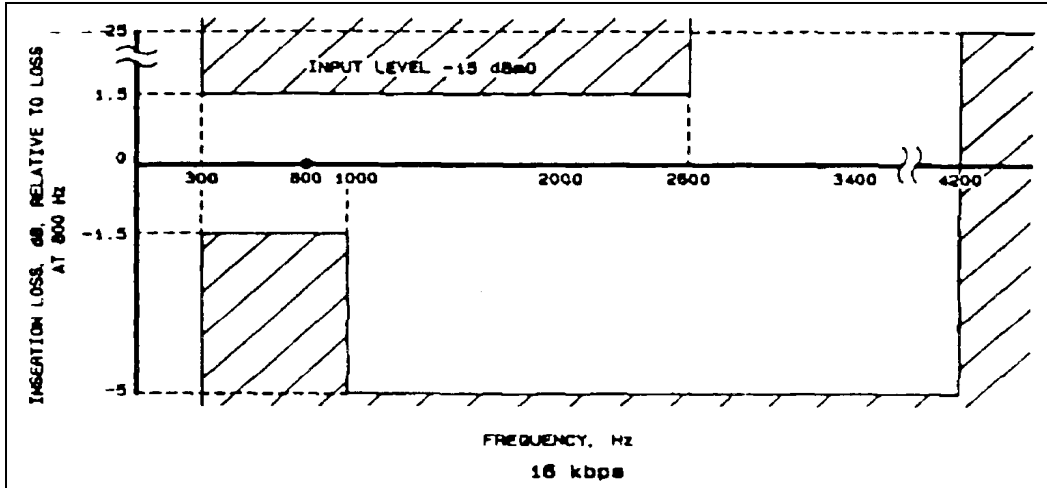| Table A-2. Insertion Loss Limits for CVSD		
Rate (kbps)	**Frequency (f) (Hz)**	**Insertion Loss (dB) (Referenced to 800 Hz)**
16	$f < 300$	≥ -1.5
	$300 \leq f \geq 1000$	-1.5 to 1.5
	$1000 \leq f \geq 2600$	-5 to 1.5
	$2600 \leq f \geq 4200$	≥ -5
	$4200 \leq f$	≥ 25
32	$f < 300$	≥ -1
	$300 \leq f \geq 1400$	-1 to 1
	$1400 \leq f \geq 2600$	3 to 1
	$2600 \leq f \geq 3400$	3 to 2
	$3400 \leq f \geq 4200$	≥ -3
	$4200 \leq f$	≥ 25

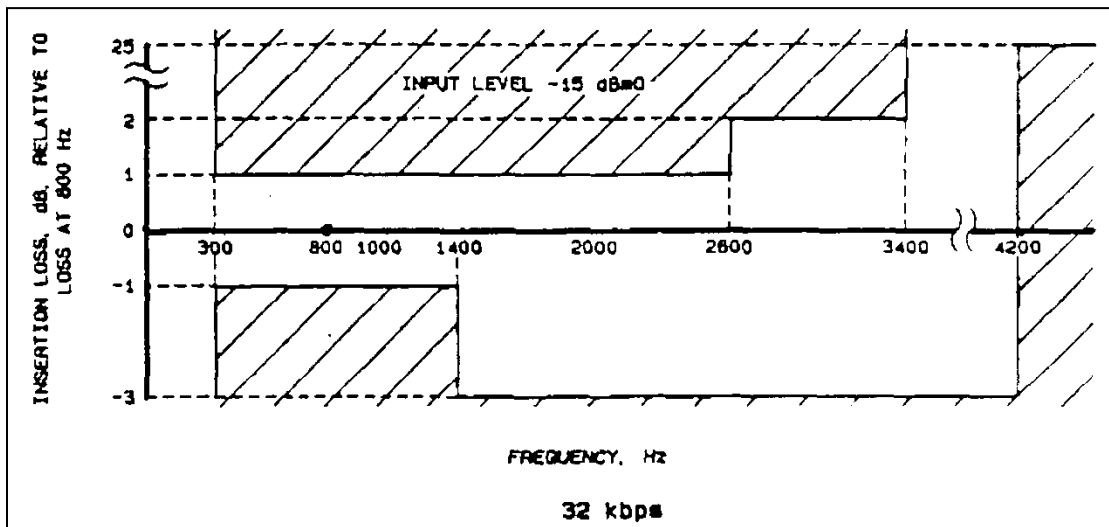Figure A-5.   Insertion Loss vs. Frequency for CVSD (16 kbps)

Figure A-6.   Insertion Loss vs. Frequency for CVSD (32 kbps)

A.5.j(4)   Variation of Gain With Input Level

The variation in output level, relative to the value at −15 dBm0 input, shall be within the limits of Figure A-7 and Figure A-8 for an input frequency of 800 Hz ±10.
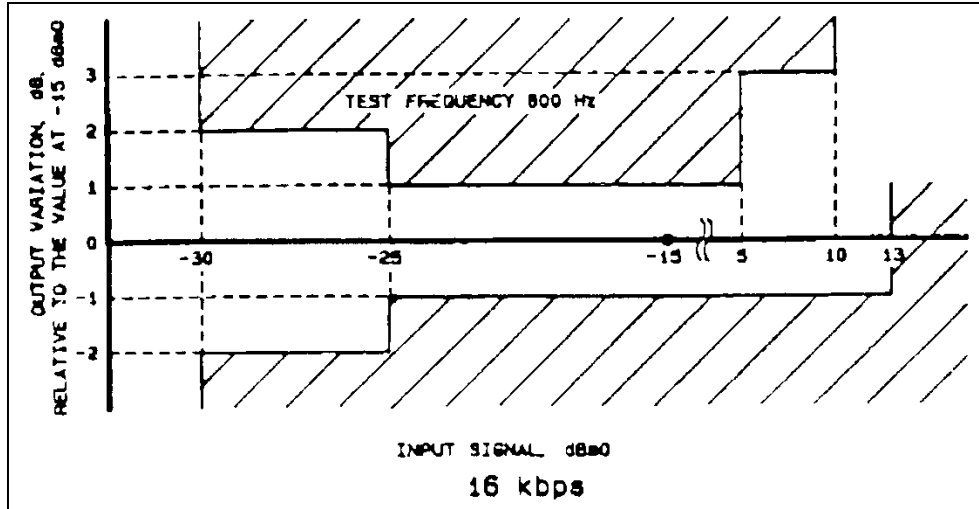
Figure A-7.   Variation of Gain with Input Level for CVSD (16 kbps)
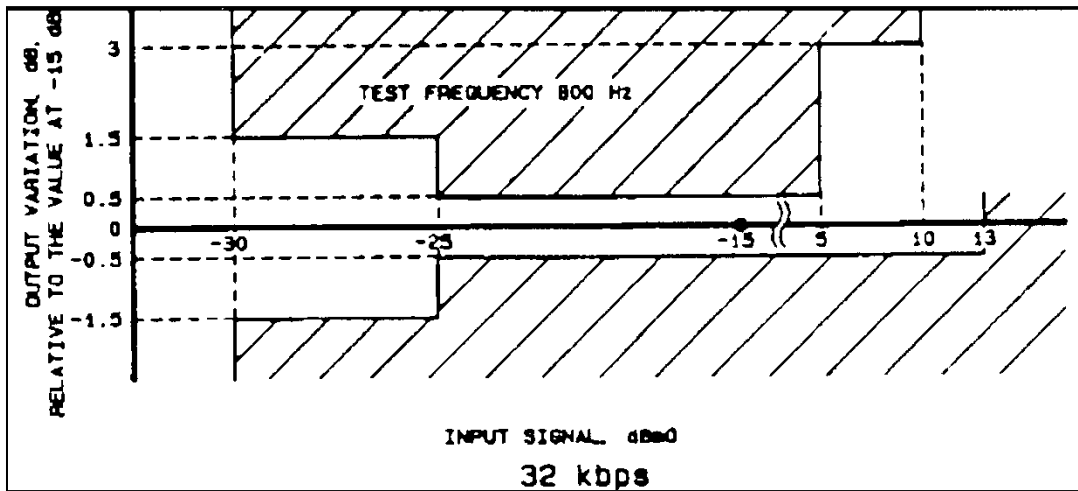

Figure A-8.   Variation of Gain With Input Level for CVSD (32 kbps)

A.5.j(5)   Idle Channel Noise

The idle channel noise shall not exceed the limits shown in Table A-3 when measured at the CVSD decoder output.

Table A-3. Idle Channel Noise Limits for CVSD	
Data Signaling Rate (kbps)	Idle Channel Noise (dBm0)
16	−40
32	−50

A.5.j(6)   Variation of Quantizing Noise With Input Level

The minimum signal to quantizing noise ratio over the input signal level range shall be above the limits of Figure A-9 and Figure A-10. The noise ratio shall be measured with flat weighting (unweighted) at the decoder output with a nominal 800-Hz ±10 sine wave test signal at the encoder input.
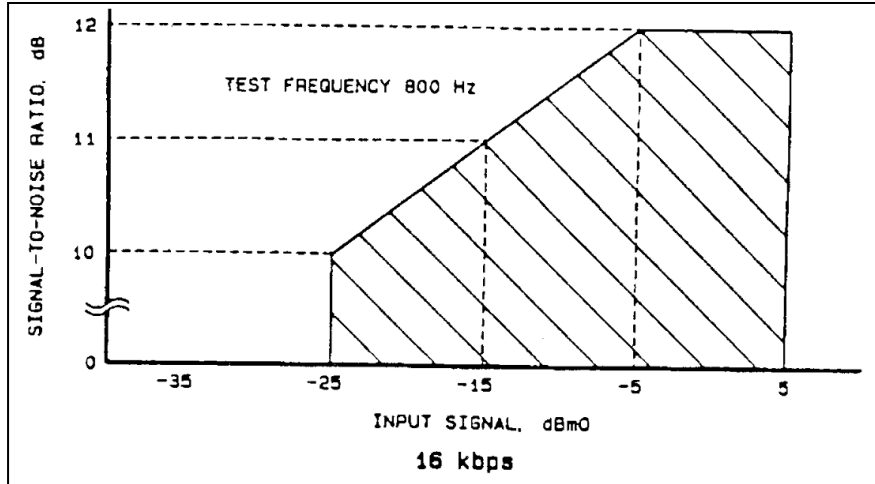
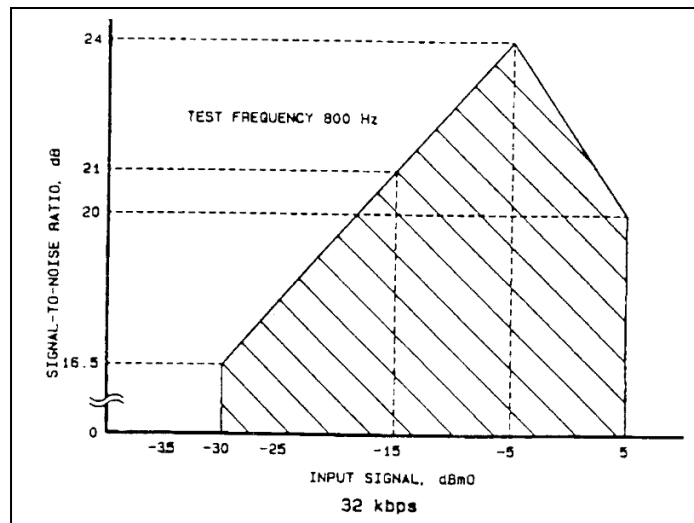Figure A-9.   Signal to Quantizing Noise Ratio vs. Input Level for CVSD (16 kbps)

Figure A-10.   Signal to Quantizing Noise Ratio vs. Input Level for CVSD (32 kbps)

A.5.j(7)   Variation of Quantizing Noise With Frequency

The minimum signal to quantizing noise ratio over the input frequency range shall be above the limits of Figure A-11 and Figure A-12. The noise ratio shall be measured with flat weighting (unweighted) at the decoder output with a sine wave test signal of −15 dBm0.
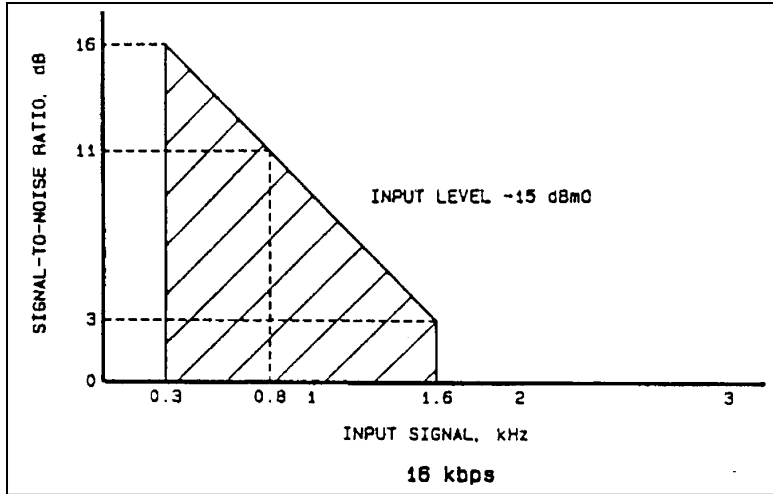
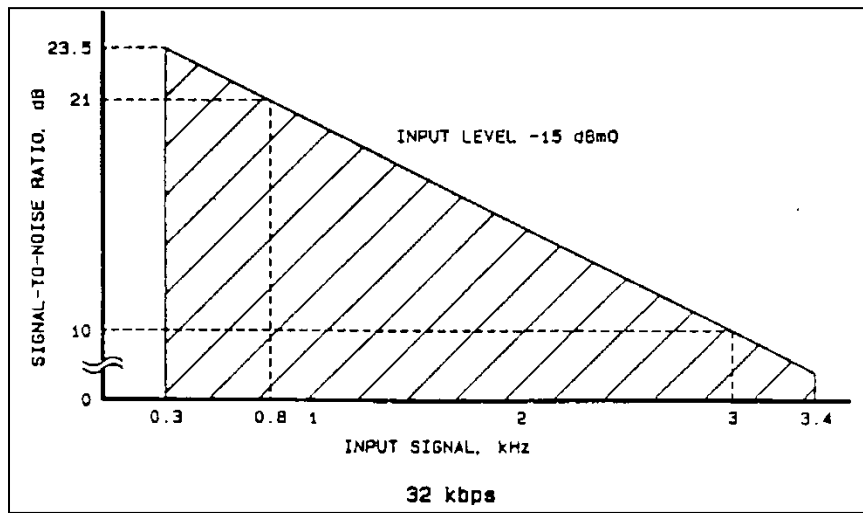Figure A-11.   Signal to Quantizing Noise Ratio vs. Frequency for CVSD (16 Kbps)

Figure A-12.   Signal to Quantizing Noise Ratio vs. Frequency for CVSD (32 Kbps)

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APPENDIX 5-B

Citations

Daniel T. Laird. Voice encode/decode subsystem in a system for acquisition of test data using pulse code modulation. US Patent 5,557,635, filed September 28, 1994 and issued September 17, 1996.

**** END OF CHAPTER 5 ****