

## APPENDIX F

### Continuously Variable Slope Delta Modulation

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## Acronyms

CVSD	continuously variable slope data
dB	decibel
Hz	hertz
kbps	kilobits per second
ms	microsecond
PAM	pulse amplitude modulator

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## APPENDIX F

### Continuously Variable Slope Delta Modulation

#### 1.0 General

The continuously variable slope delta (CVSD) modulation is a nonlinear, sampled data, feedback system which accepts a band-limited analog signal and encodes it into binary form for transmission through a digital channel. At the receiver, the binary signal is decoded into a close approximation of the original analog signal. A typical CVSD converter consisting of an encoder and decoder is shown in [Figure F-1](#) and [Figure F-2](#).

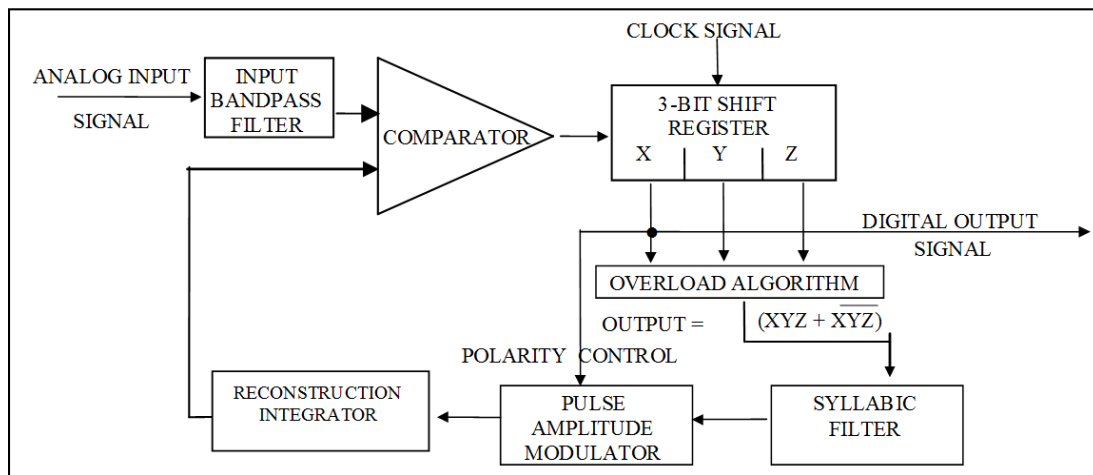


Figure F-1. Typical CVSD Encoder

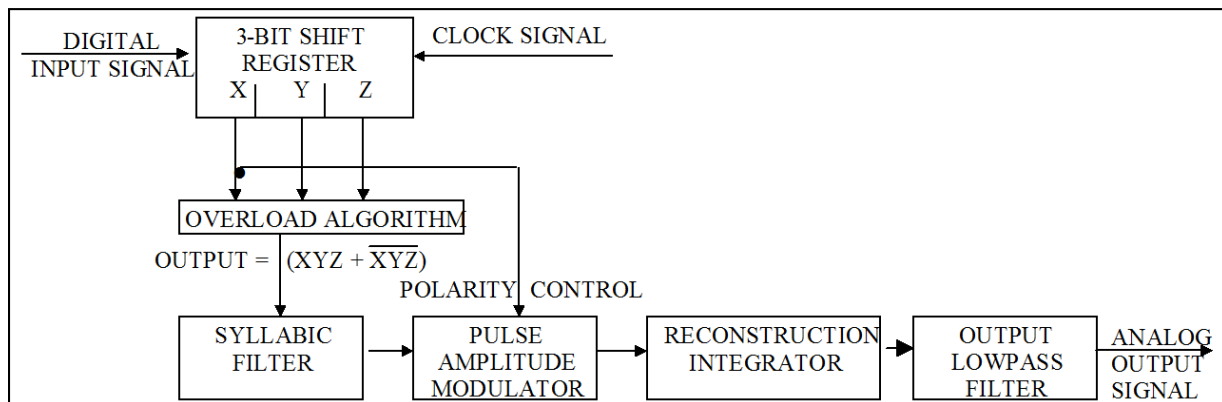


Figure F-2. Typical CVSD Decoder

#### 2.0 General Descriptions

A general description of the delta modulation and the CVSD converter can be found in the following subparagraphs.

##### 2.1 Delta Modulation

Delta modulation is an A-D conversion technique resulting in a form of digital pulse modulation. A delta modulator periodically samples the amplitude of a band-limited analog

signal, and the amplitude differences of two adjacent samples are coded into n-bit code words. This nonlinear, sampled-data feedback system then transmits the encoded bit stream through a digital channel. At the receiving end, an integrating network converts the delta-modulated bit stream through a decoding process into a close approximation of the original analog signal.

## 2.2 CVSD Converter

A typical CVSD converter consists of an encoder and a decoder (see [Figure F-1](#) and [Figure F-2](#)). The analog input signal of the CVSD encoder is band-limited by the input band, pass filter. The CVSD encoder compares the band-limited analog input signal with an analog feedback approximation signal generated at the reconstruction integrator output. The digital output signal of the encoder is the output of the first register in the “run-of-three” counter. The digital output signal is transmitted at the clock (sample) rate and will equal “1” if the analog input signal is greater than or equal to the analog feedback signal at the instant of sampling. For this value of the digital output signal, the pulse amplitude modulator (PAM) applies a positive feedback pulse to the reconstruction integrator; otherwise, a negative pulse is applied. This function is accomplished by the polarity control signal, which is equal to the digital encoder output signal. The amplitude of the feedback pulse is derived by means of a 3-bit shift register, logic sensing for overload, and a syllabic lowpass filter. When a string of three consecutive ones or zeros appears at the digital output, a discrete voltage level is applied to the syllabic filter, and the positive feedback pulse amplitude increases until the overload string is broken. In such an event, ground potential is fed to the filter by the overload algorithm, forcing a decrease in the amplitude of the slope voltage out of the syllabic filter. The encoder and decoder have identical characteristics except for the comparator and filter functions.

The CVSD decoder consists of the input band pass filter, shift register, overload algorithm, syllabic filter, PAM and reconstruction integrator used in the encoder, and an output low-pass filter. The decoder performs the inverse function of the encoder and regenerates speech by passing the analog output signal of the reconstruction integrator through the low-pass filter. Other characteristics optimize the CVSD modulation technique for voice signals. These characteristics include the following.

- a. Changes in the slope of the analog input signal determine the step-size changes of the digital output signal.
- b. The feedback loop is adaptive to the extent that the loop provides continuous or smoothly incremental changes in step size.
- c. Companding is performed at a syllabic rate to extend the dynamic range of the analog input signal.
- d. The reconstruction integrator is of the exponential (leaky) type to reduce the effects of digital errors.

## 3.0 **Detailed Descriptions**

The characteristics described in subparagraphs [3.1](#) through [3.9](#) are in addition to those specified in Section [5.0](#) and are for guidance only.

### 3.1 Input Band Pass Filter

The input filter provides band-limiting and is typically a second- or higher-order filter (see [Figure F-1](#)).

### 3.2 Comparator

The comparator compares the band-limited analog input signal from the filter with the output signal of the reconstruction integrator (see [Figure F-1](#)). This comparison produces the digital error signal input to the 3-bit shift register. The transfer characteristic of the comparator is such that the difference between the two input signals causes the output signal to be driven to saturation in the direction of the sign of the difference.

### 3.3 3-Bit Shift Register

The 3-bit shift register acts as a sampler which clocks the digital error signal from the comparator at the specified data signaling rate and stores the current samples and two previous samples of the error signal (see [Figure F-1](#) and [Figure F-2](#)). The digital output signal is a binary signal having the same polarity as the input signal from the comparator at the time of the clock signal. The digital output signal is also the digital output of the encoder and is referred to as the baseband signal. Further processing for transmission such as conditioned diphas modulation may be applied to the baseband signal. It is necessary that the inverse of any such processing be accomplished and the baseband signal restored before the CVSD decoding process is attempted.

### 3.4 Overload Algorithm

The overload algorithm operates on the output of the 3-bit shift register ( $X, Y, Z$ ) using the run-of-threes coincidence algorithm so that the algorithm output equals  $(XYZ + \overline{XYZ})$  (see [Figure F-1](#) and [Figure F-2](#)). The output signal is a binary signal at the clock signaling rate and is true for one clock period following the detection of three like bits and false at all other times.

### 3.5 Syllabic Filter

The syllabic filter acts as a low-pass filter for the output signal from the overload algorithm (see [Figure F-1](#) and [Figure F-2](#)). The slope-voltage output of the syllabic filter is the modulating input to the PAM. The step-function response of the syllabic filter is related to the syllabic rate of speech, is independent of the sampling rate, and is exponential in nature. When the overload algorithm output is true, a charging curve is applicable. When this output is false, a discharging curve is applicable.

### 3.6 Pulse Amplitude Modulator

The PAM operates with two input signals: the output signal from the syllabic filter and the digital signal from the 3-bit shift register (see [Figure F-1](#) and [Figure F-2](#)). The syllabic filter output signal determines the amplitude of the PAM output signal and the signal from the 3-bit shift register is the polarity control that determines the direction, plus or minus, of the PAM output signal. The phrase “continuously variable” in CVSD is derived from the way the PAM output signal varies almost continuously.

### 3.7 Reconstruction Integrator

The reconstruction integrator operates on the output signal of the PAM to produce an analog feedback signal to the comparator (or an output signal to the output low-pass filter in the receiver) that is an approximation of the analog input signal (see [Figure F-1](#) and [Figure F-2](#)).

### 3.8 Output Low-Pass Filter

The output filter is a low-pass filter having a frequency response that typically has an asymptotic rolloff with a minimum slope of 40 decibels (dB) per octave, and a stopband rejection that is 45 dB or greater (see [Figure F-2](#)). The same output filter characteristic is used for encoder digital output signals of either 16 or 32 kilobits per second (kbps).

### 3.9 Typical CVSD Decoder Output Envelope Characteristics

For a resistance/capacitance circuit in the syllabic filter with time constants of 5 microseconds (ms) for both charging and discharging, the envelope characteristics of the signal at the decoder output are shown in [Figure F-3](#). For the case of switching the signal at the decoder input from the 0 percent run-of-threes digital pattern to the 30 percent run-of-threes digital pattern, the characteristic of the decoder output signal follows the resistance/capacitance charge curve. Note that the number of time constants required to reach the 90 percent charge point is 2.3, which gives a nominal charge time of 11.5 ms.

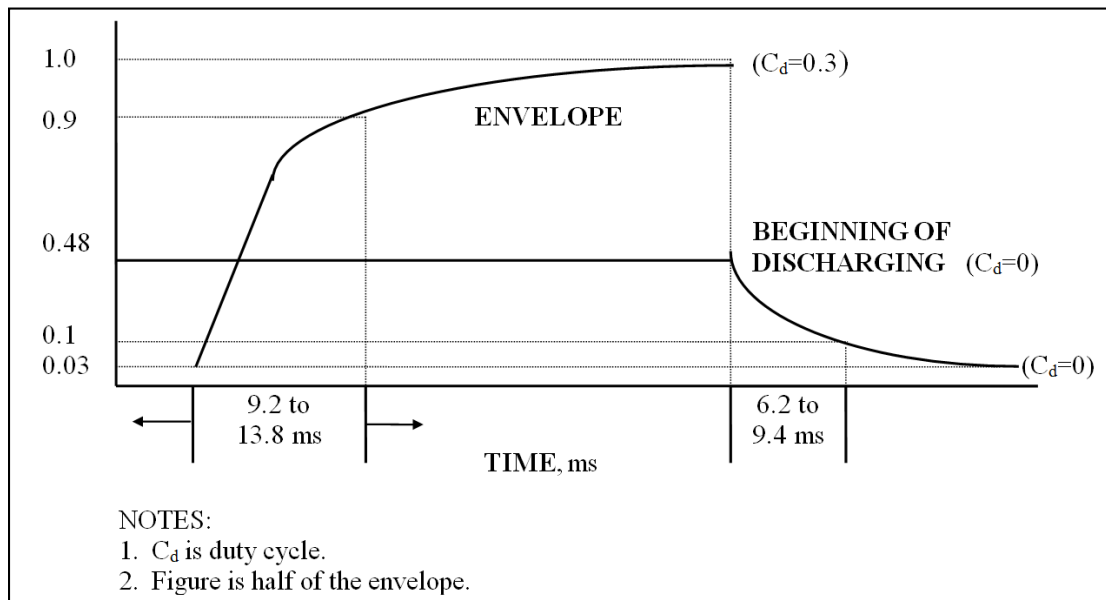


Figure F-3. Typical Envelope Characteristics of the Decoder Output Signal for CVSD

When switching the other way (from the 30 percent pattern to the 0 percent pattern), the amplitude at the beginning of discharging is, at the first moment of switching, higher (by a factor of 16) than the final value which is reached asymptotically. The final value equals  $-24$  dBm0, that is, 0.03. Therefore, the amplitude at the beginning of discharging is 0.48 (percent run-of-threes = 0). Note that the number of time constants required to reach the 10 percent point on the discharge curve is 1.57, which gives a nominal discharge time of 7.8 ms.



#### 4.0 Reference Level

The decoder analog output level with the 16 and 32 kbps, 30 percent run-of-threes reference digital pattern applied to the decoder input shall be the reference level for the CVSD requirements of this standard and shall be designated 0 dBm0 (see Subparagraph [5.9.1](#)).

#### 5.0 CVSD Characteristics

The characteristics of CVSD are described in the following subparagraphs.

##### 5.1 Input and Output Impedances


The analog input and output impedances for CVSD converters are not standardized. These impedances depend upon the application of the converters.

##### 5.2 Data Signaling Rates

The CVSD converter shall be capable of operating at 16 and 32 kbps.

##### 5.3 Input and Output Filters

The analog input shall be band pass filtered. The analog output shall be low pass filtered.

 <p><b>NOTE</b></p>	<p>Details of input and output filters, consistent with the CVSD performance requirements of this standard, will be determined in applicable equipment specifications based on validated requirements</p>
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##### 5.4 Overload Algorithm

A 3-bit shift register shall be used for the CVSD encoder and decoder (see [Figure F-1](#) and [Figure F-2](#)). The overload logic shall operate on the output of this shift register using the run-of-threes coincidence algorithm. The algorithm output signal shall be a binary signal at the data-signaling rate. This signal shall be true for one clock period following the detection of three like bits (all 0s or all 1s) and false at all other times.

##### 5.5 Compression Ratio

The compression ratio shall be nominally 16:1 with a maximum of 21:1 and a minimum of 12:1. The maximum slope voltage shall be measured at the output of the syllabic filter for a 30 percent run-of-threes digital pattern. The minimum slope voltage shall be measured at the output of the syllabic filter for a 0 percent run-of-threes digital pattern.

##### 5.6 Syllabic Filter

The syllabic filter shall have a time constant of 5 ms  $\pm$ 1. The step function response of the syllabic filter shall be exponential in nature. When the output of the overload algorithm is true, a charge curve shall be applicable. When the output of the overload algorithm is false, a discharge curve shall be applicable.

##### 5.7 Reconstruction Integrator Time Constant

The reconstruction integrator shall have a time constant of 1 ms  $\pm$ 0.25.

5.8 Analog-to-Digital Conversion

An 800-Hertz (Hz)  $\pm 10$  signal at a 0 dBm0 level applied to the input of the encoder shall give a duty cycle of 0.30 at the algorithm output of the encoder shown in [Figure F-1](#).

5.9 Digital-to-Analog Conversion

The characteristics of a digital-to-analog conversion are described in the following subparagraphs.

5.9.1 Relation of Output to Input

With the applicable reference digital patterns of [Table F-1](#) applied to the digital input of the decoder as shown in [Figure F-4](#), the analog output signal shall be 800 Hz  $\pm 10$  at the levels shown in [Table F-1](#), measured at the decoder output. These digital patterns, shown in hexadecimal form, shall be repeating sequences.

<b>Table F-1. Decoder Reference Digital Patters for CVSD</b>			
Data Signaling Rate (kbps)	Digital Pattern	Run-of-threes (percent)	Output (dBm0)
16	DB492	0	$-24 \pm 1$
32	DB54924AB6	0	$-24 \pm 1$
16	FB412	30	$0 \pm 1$
32	FDA A10255E	30	$0 \pm 1$

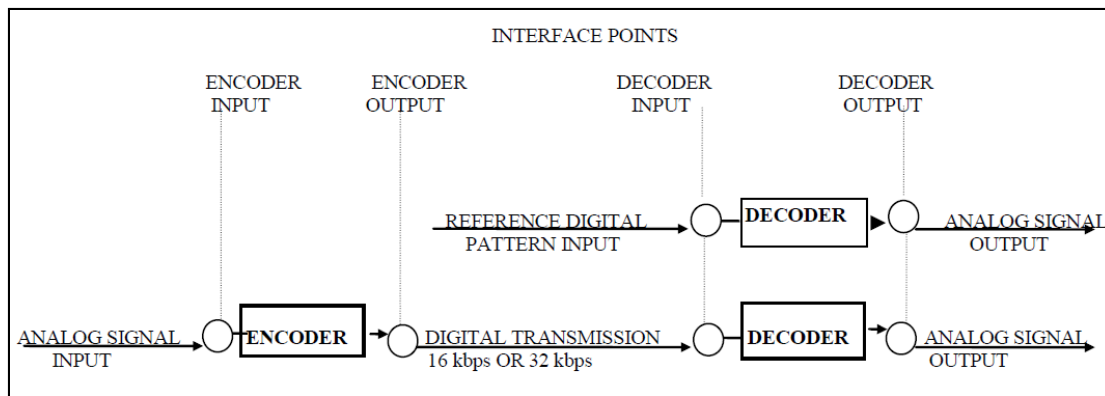



Figure F-4. Interface Diagram for CVSD Converter

5.9.2 Conversion Speed

When the decoder input is switched from the 0 percent run-of-threes digital pattern to the 30 percent run-of-threes digital pattern, the decoder output shall reach 90 percent of its final value within 9 to 14 ms. When the decoder input is switched from the 30 percent run-of-threes digital pattern to the 0 percent run-of-threes digital pattern, the decoder output shall reach 10 percent of the 30 percent run-of-threes value within 6 to 9 ms. These values shall apply to both the 16- and 32-kbps data signaling rates.

### 5.10 CVSD Converter Performance

The characteristics specified in subparagraphs [5.10.1](#) through [5.10.7](#) apply to one CVSD conversion process obtained by connecting the output of an encoder to the input of a decoder (see [Figure F-4](#)).

 <p><b>NOTE</b></p>	<p>Test signal frequencies that are submultiples of the data signaling rate shall be avoided by offsetting the nominal test frequency slightly; for example, an 800-Hz test frequency could be offset to 804 Hz. This test frequency offset will avoid nonlinear distortion, which can cause measurement difficulties when CVSD is in tandem with pulse code modulation.</p>
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#### 5.10.1 Companding Speed

When an 800-Hz  $\pm 10$  sine wave signal at the encoder input is switched from  $-24$  dBm0 to 0 dBm0, the decoder output signal shall reach 90 percent of its final value within 9 to 14 ms.

#### 5.10.2 Insertion Loss

The insertion loss between the encoder input and the decoder output shall be 0 dB  $\pm 2$  dB with an 800 Hz  $\pm 10$ , 0 dBm0 input to the encoder.

#### 5.10.3 Insertion Loss vs. Frequency Characteristics

The insertion loss between the encoder input and decoder output, relative to 800 Hz  $\pm 10$  measured with an input level of  $-15$  dBm0 applied to the converter input, shall not exceed the limits indicated in [Table F-2](#) and shown in [Figure F-5](#) and [Figure F-6](#).

<b>Table F-2. Insertion Loss Limits for CVSD</b>		
<b>Rate (kbps)</b>	<b>Frequency (f) (Hz)</b>	<b>Insertion Loss (dB) (Referenced to 800 Hz)</b>
16	$f < 300$	$\geq -1.5$
	$300 \leq f \leq 1000$	-1.5 to 1.5
	$1000 \leq f \leq 2600$	-5 to 1.5
	$2600 \leq f \leq 4200$	$\geq -5$
	$4200 \leq f$	$\geq 25$
32	$f < 300$	$\geq -1$
	$300 \leq f \leq 1400$	-1 to 1
	$1400 \leq f \leq 2600$	3 to 1
	$2600 \leq f \leq 3400$	3 to 2
	$3400 \leq f \leq 4200$	$\geq -3$
$4200 \leq f$	$\geq 25$	

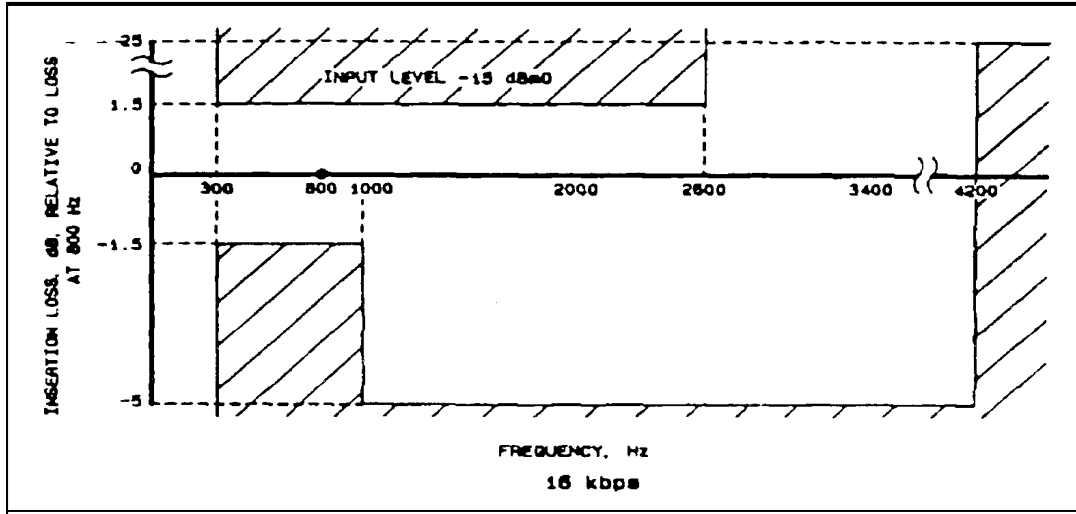


Figure F-5. Insertion Loss vs. Frequency for CVSD (16 kbps)

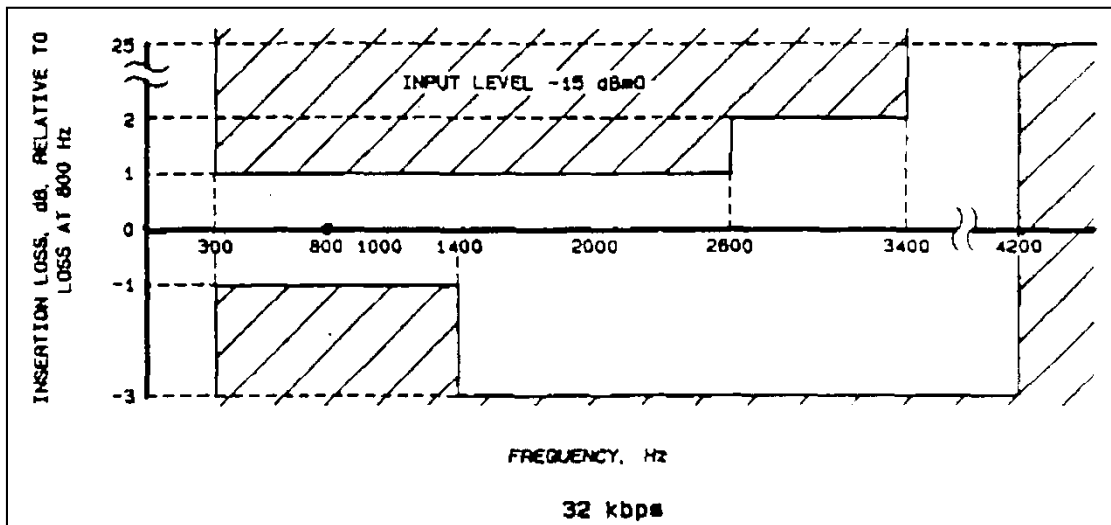


Figure F-6. Insertion Loss vs. Frequency for CVSD (32 kbps)

#### 5.10.4 Variation of Gain With Input Level

The variation in output level, relative to the value at  $-15$  dBm0 input, shall be within the limits of [Figure F-7](#) and [Figure F-8](#) for an input frequency of  $800$  Hz  $\pm 10$ .

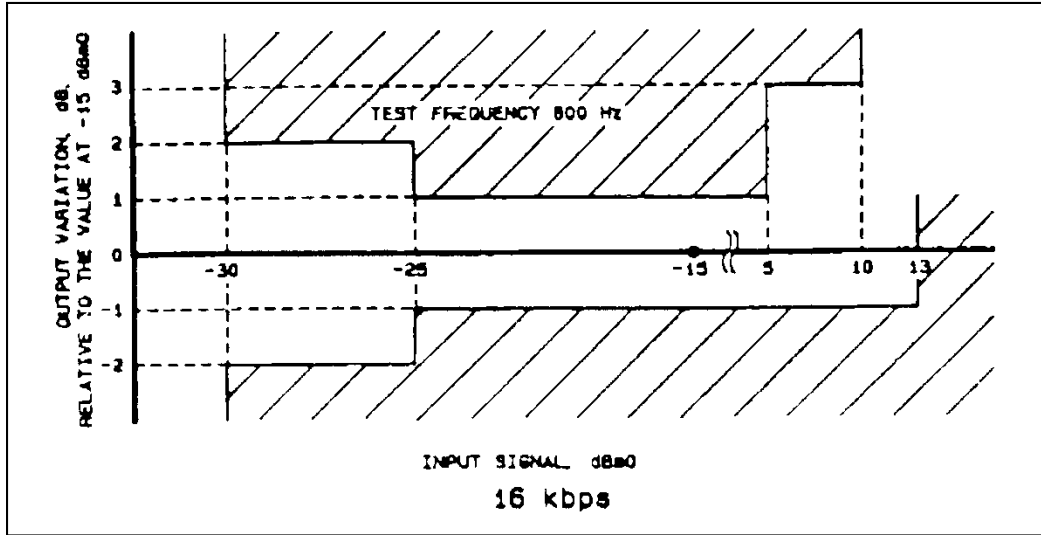


Figure F-7. Variation of Gain With Input Level for CVSD (16 kbps)

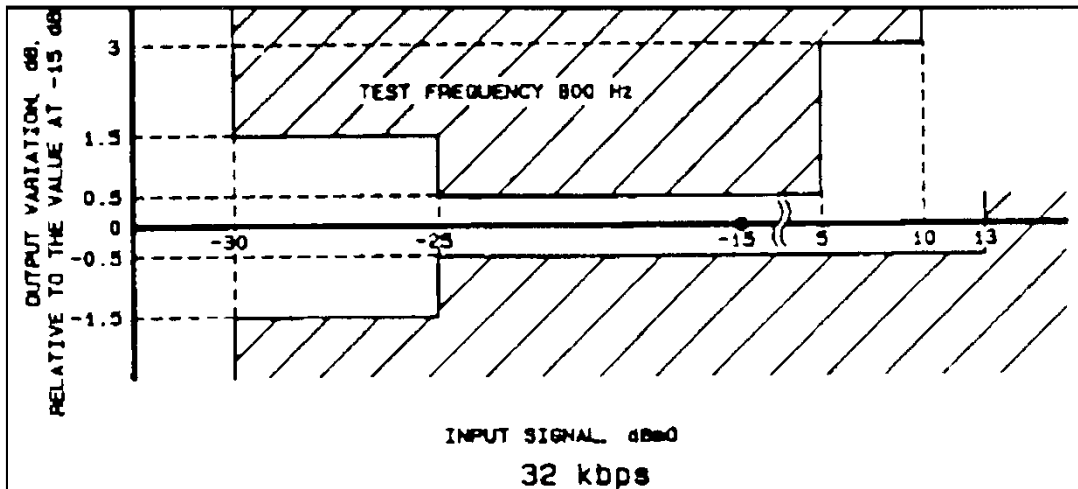


Figure F-8. Variation of Gain With Input Level for CVSD (32 kbps)

5.10.5 Idle Channel Noise

The idle channel noise shall not exceed the limits shown in [Table F-3](#) when measured at the CVSD decoder output.

<b>Table F-3. Idle Channel Noise Limits for CVSD</b>	
Data Signaling Rate (kbps)	Idle Channel Noise (dBm0)
16	-40
32	-50

5.10.6 Variation of Quantizing Noise With Input Level

The minimum signal to quantizing noise ratio over the input signal level range shall be above the limits of [Figure F-9](#) and [Figure F-10](#). The noise ratio shall be measured with flat weighting (unweighted) at the decoder output with a nominal 800-Hz  $\pm 10$  sine wave test signal at the encoder input.

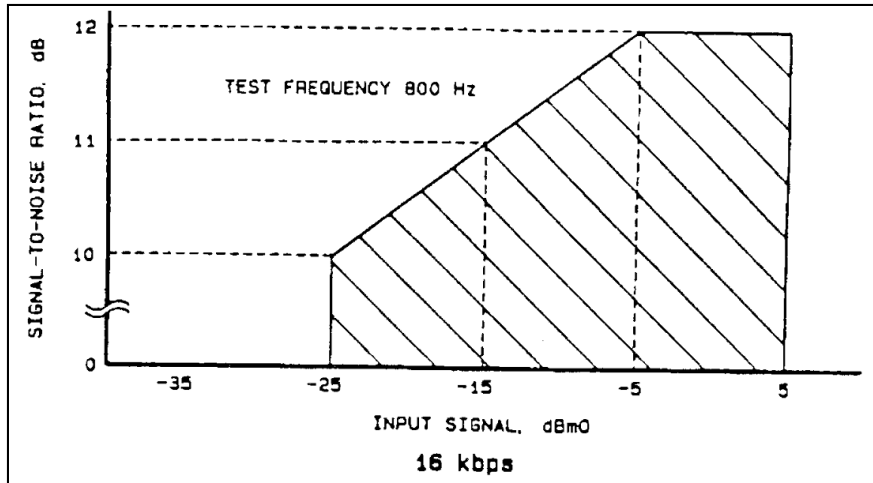


Figure F-9. Signal to Quantizing Noise Ratio vs. Input Level for CVSD (16 kbps)

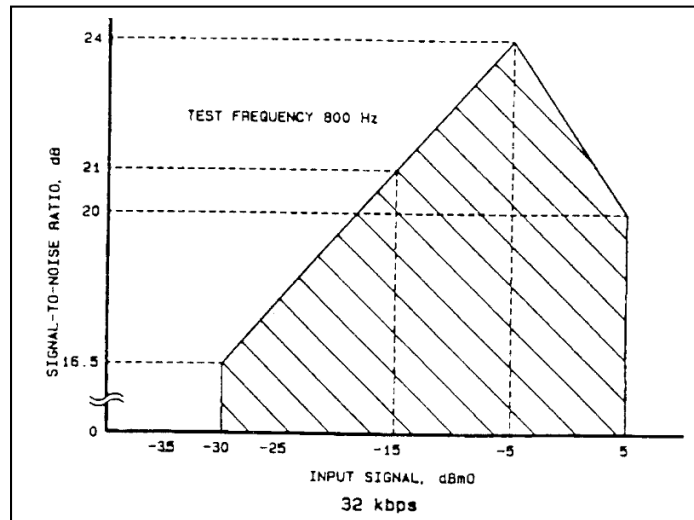


Figure F-10. Signal to Quantizing Noise Ratio vs. Input Level for CVSD (32 kbps)

#### 5.10.7 Variation of Quantizing Noise With Frequency

The minimum signal to quantizing noise ratio over the input frequency range shall be above the limits of [Figure F-11](#) and [Figure F-12](#). The noise ratio shall be measured with flat weighting (unweighted) at the decoder output with a sine wave test signal of  $-15$  dBm0.

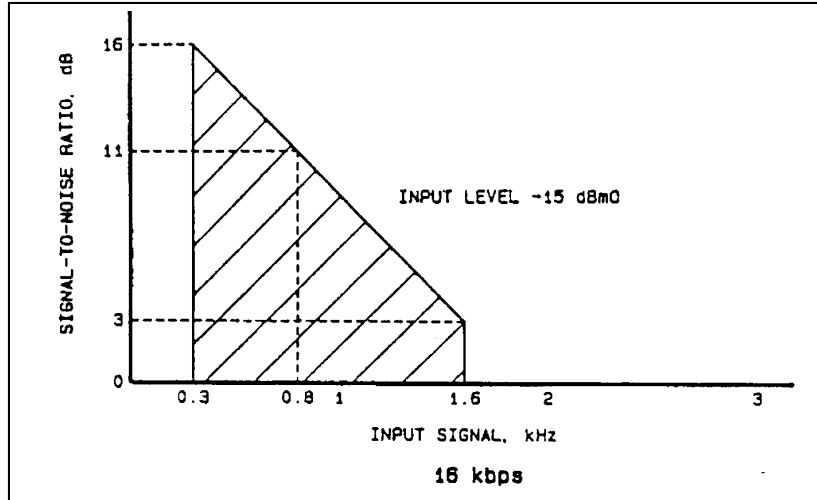


Figure F-11. Signal to Quantizing Noise Ratio vs. Frequency for CVSD (16 Kbps)

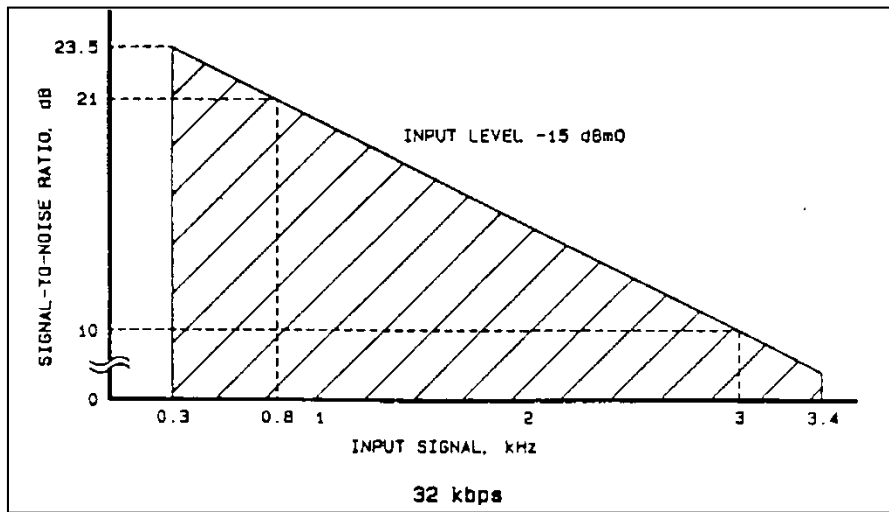


Figure F-12. Signal to Quantizing Noise Ratio vs. Frequency for CVSD (32 Kbps)

**\*\*\*\* END OF APPENDIX F \*\*\*\***